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Project Whirlwind
Servomechanisms Laboratory
Massachusetts Institute of Technology
Cambridge, Massachusetts

SUBJECT: **PRELIMINARY TESTS ON THE FOUR-CORE MAGNETIC-MEMORY ARRAY**

To: 6345 Engineers

From: W. N. Papian

Date: June 18, 1951

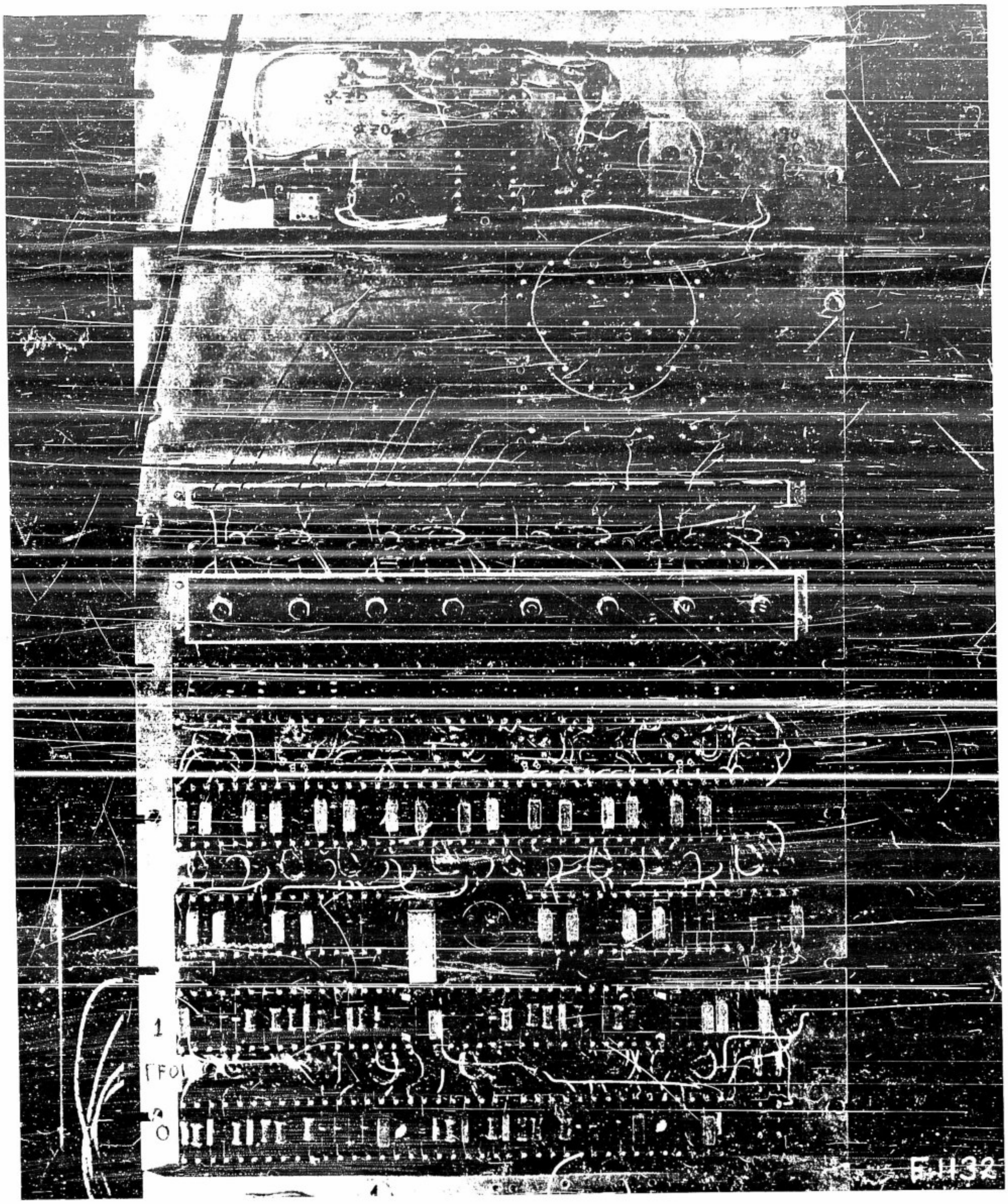
Abstract: Successful operation of a four-core magnetic-memory array indicates the soundness of a multi-coordinate storage and selection scheme. The ability of one core to retain information in the face of an unlimited amount of disturbing activity was tested, and current-variation margins determined.

Brief Description

A four-core magnetic-memory array was built to demonstrate the principle of multi-coordinate storage and selection. It consists of four cores arranged in a square, with cores selected by the choice of x and y coordinates. The windings which determine whether a binary ONE or ZERO is written in the selected core are, like the sensing windings, connected together in the four-core plane and act, to some extent, like a z coordinate of a three-coordinate array.

The surrounding equipment consists of some more-or-less standard test equipment, two specially built panels containing the x and y flip-flops and the gating and driving circuitry associated with the coordinate axes, and some miscellaneous panels adapted for this problem. Figure 1 is a photograph of the cores and part of the rest of the equipment.

Two basic modes of operation have been tried. The first, in which an information pattern was cycled indefinitely around the four cores, was successfully run but has been abandoned in favor of the present mode. The operating mode now in use resembles an elementary spot-interaction test as used by the storage-tube group. It consists of writing a binary digit in a given core, then operating around the other cores for a large number of cycles in a manner intended to "disturb" (tending to destroy) that information, finally returning to read the contents of the given core. This mode has also been run successfully.



FOUR CORE, TWO-DIMENSIONAL
MAGNETIC MEMORY TEST SETUP

FIG. 1

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Logical Design

In the logical layout of the equipment as used in the first basic mode of operation, a given information pattern was cycled around the four cores. It was possible for the oscilloscope to "look at" the sensing output from the array (or any portion of the array) (1) each time a selected piece of information was being handled, or (2) each time a selected core handled information. The piece of information in (1), or the core in (2), could be selected by push button while any pattern of information was cycling around the array.

The limited value of a test which renews the information in a core after only two or three disturbances (caused by activity elsewhere in the array) made it desirable to drop this first basic operating mode (information cycling) and subject the cores, instead, to a spot-interaction type of test which assessed their ability to retain information in the face of an unlimited amount of disturbance.

Refer to Figure 2 (by R. P. Mayer) for the present scheme of operation. With the switch positions as shown, the setup is ready to test the ability of core 00 to hold a ONE. The multivibrator frequency divider is allowed to run free and becomes a source of synchronous high- and low-frequency pulses. After corrective short time delays, the pulses are fed into the system. The low-frequency pulse first goes to gate and delay unit 3a and thence to trigger the oscilloscope. It then passes through coder 1 to preset flip-flops 1, 2, 3, 5, and 6 to ZERO, ZERO, ZERO, ONE, and ZERO respectively. The first of the block of high-frequency pulses emanating from the pulse-block former passes through switch 2 and gate 2 and sets FF4 to a ZERO. One read-write cycle is performed on core 00 from read-write control (gate 8 is on), after which FF3 is set to a ONE (turning off gate 8), to remain that way until the major cycle is over and another low-frequency pulse comes along. The skip circuit sees to it that core 00 is not selected again for the rest of the major cycle, and gate 8 prevents any writing activity for the same period. The opening of switch 7 momentarily during operation ensures that a ONE is written into core 00. This core may be selected either once for every low-frequency pulse (once each major cycle - binary counter set to 2^0), every 2 or 4 major cycles (binary counter set to 2^1 or 2^2), or once each time a button on the push button synchronizer is pushed (switch 1 open).

The ability of core 00 to hold a ZERO is tested by reversing switches 2 and 3 and momentarily closing switch 6 during operation. The selected test core may be other than 00, as determined by the settings of switches 4 and 5.

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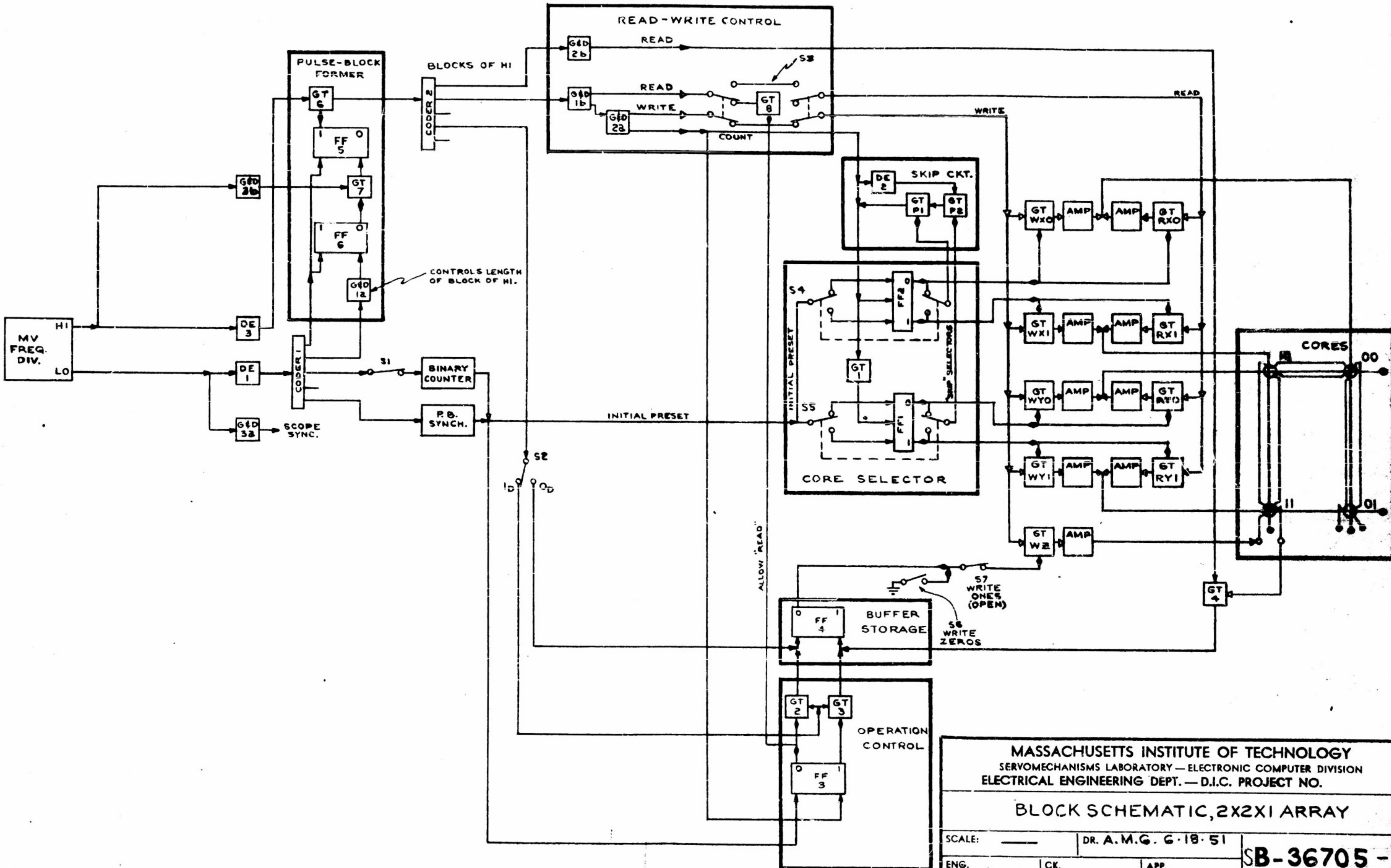

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
SERVOMECHANISMS LABORATORY — ELECTRONIC COMPUTER DIVISION
ELECTRICAL ENGINEERING DEPT. — D.I.C. PROJECT NO.

BLOCK SCHEMATIC, 2X2X1 ARRAY

SCALE: —	DR. A.M.G. 6·18·51	SB-36705-2
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FIG. 2

The Cores

The cores now in this array are designated as MTS 6464 by the supplier, the Allegheny Ludlum Steel Corp. They consist of 10 turns of Silectron tape 1 mil thick and 1/8 inch wide; the resultant rings have a mean length of 4.24 cm, a cross-sectional area about 0.01 sq cm, and an inside diameter of 1/2 inch. They are encased in slightly oversized plastic containers, and wound with five 25-turn windings and one 10-turn winding of #30 magnet wire.

The material Silectron is a standard electrical sheet steel with a special anneal designed to produce the B-H characteristic of Figure 3. The successful metallic core used in the experimental work on individual cores (see Report R-192) was made of the same material.

Circuitry

The 25-turn magnetizing windings on the two cores comprising one selecting coordinate are connected in series with a 100-ohm resistor as the plate load of one section of a 6AS7. The resistor makes it possible to "look at" the current flowing through the windings. A 500-ohm rheostat in the cathode circuit of the 6AS7 section is used to vary that current. The 6AS7 section is driven by one section of a 2C51 which inverts the waveform coming from the 6AS6 gate tube. Figure 4 shows one channel of the nine in use. The 6AS7 section puts from about 40 ma to just under 1/4 amp. through the core windings, depending on the cathode rheostat setting. The rise time of the current waveform is well under 1/2 microsecond; it may be lengthened by shorting the choke in the plate load of the 2C51 and adding some capacitance.

The fifth 25-turn winding on each core is the sensing winding; the four of them are connected in series-aiding to deliver the output from the array. The 10-turn windings are connected with alternating polarities for a special test.

Results and Conclusions

In general, operation was stable and with good margins.

The adjustment for optimum operation was decided in an arbitrary manner as the compromise between signal ratios and response times that seemed most promising. Figure 5 summarizes these results. It shows the effect of disturbing activity (interaction) on information retention. Disturbed-signal ratios, for different amounts of disturbance, may also be derived from these scope traces.

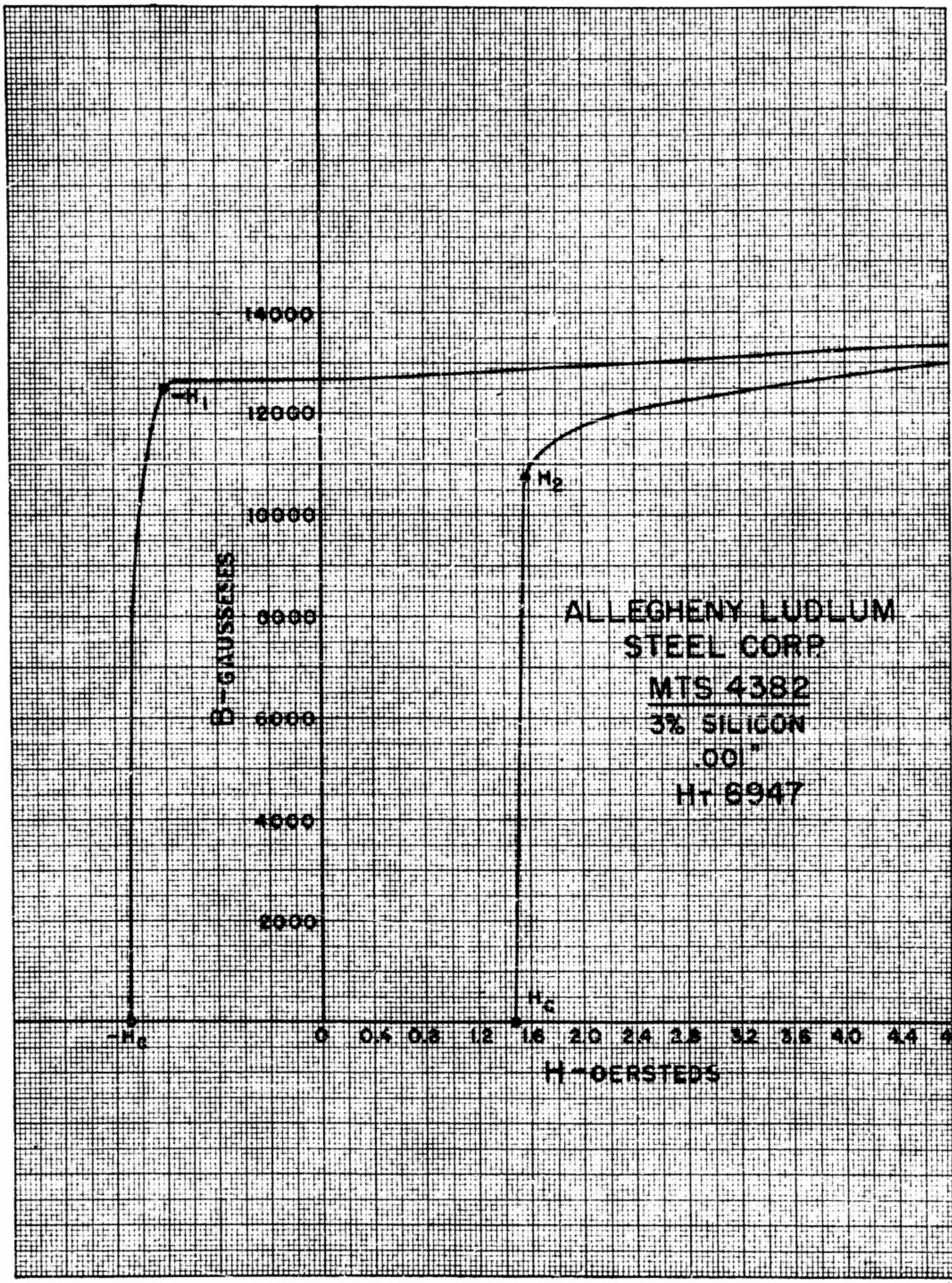

FIG. 3

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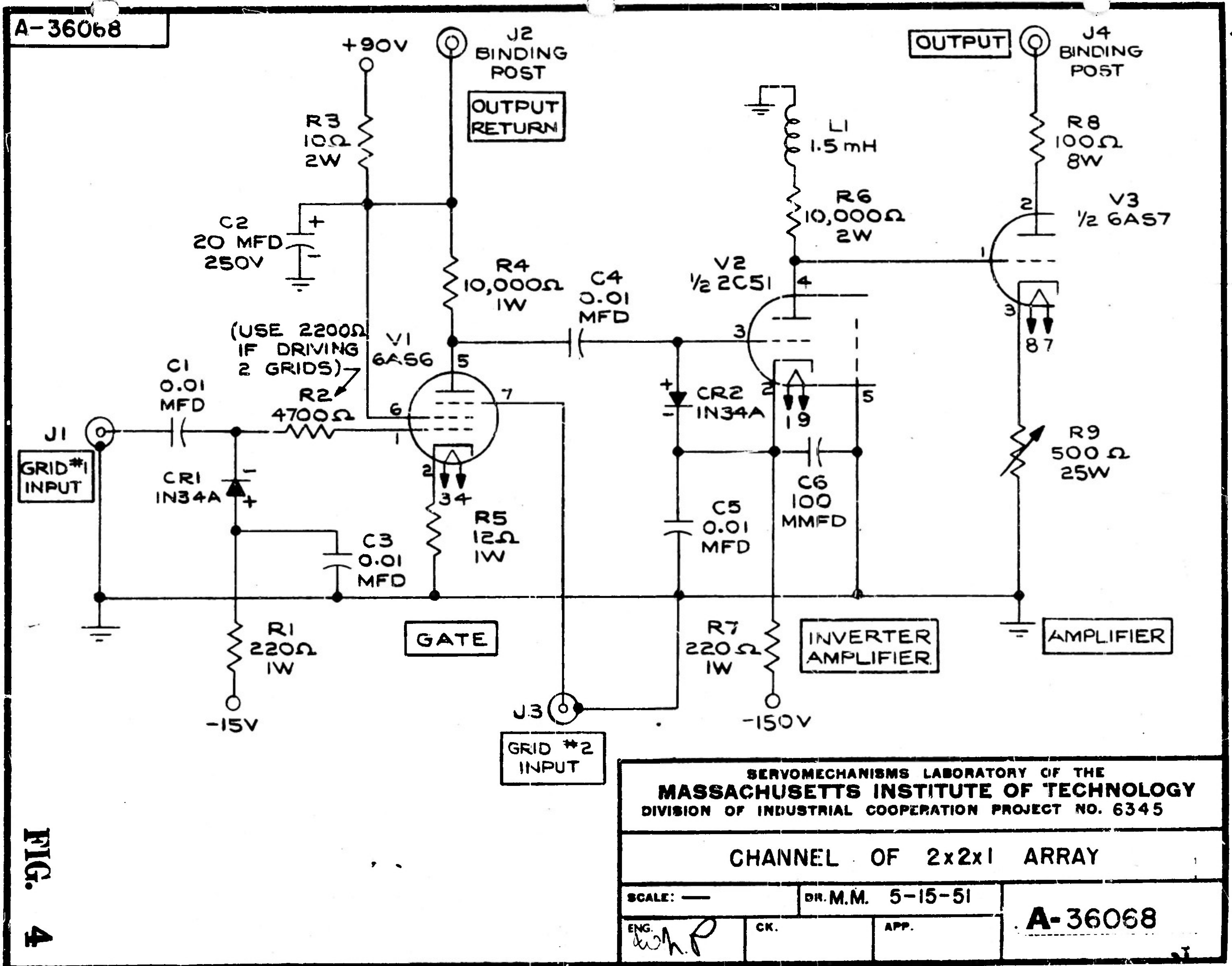
A-36068
+90V
J2
BINDING
POST
OUTPUT
RETURN
OUTPUT
J4
BINDING
POST
R3
10Ω
2W
C2
20 MFD
250V
R4
10,000Ω
1W
C4
0.01
MFD
L1
1.5 mH
R6
10,000Ω
2W
R8
100Ω
8W
V3
½ 6AS7
V2
½ 2C51
(USE 2200Ω
IF DRIVING
2 GRIDS)
V1
6AS6
C1
0.01
MFD
R2
4700Ω
J1
GRID #1
INPUT
CR1
1N34A
CR2
1N34A
R5
12Ω
1W
C3
0.01
MFD
C5
0.01
MFD
C6
100
MMFD
R9
500 Ω
25W
R1
220Ω
1W
-15V
GATE
R7
220 Ω
1W
-150V
INVERTER
AMPLIFIER
AMPLIFIER
J3
GRID #2
INPUT
SERVOMECHANISMS LABORATORY OF THE
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DIVISION OF INDUSTRIAL COOPERATION PROJECT NO. 6345
CHANNEL OF 2x2x1 ARRAY
SCALE: —
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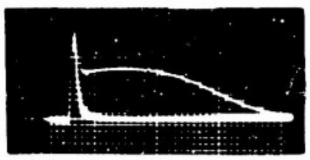
FIG. 4

(a) AFTER 0 READ CYCLES

(b) AFTER 50 READ CYCLES



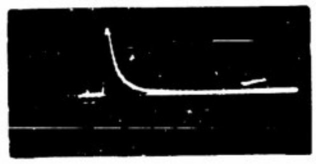
(c) AFTER 400 READ CYCLES

5μs

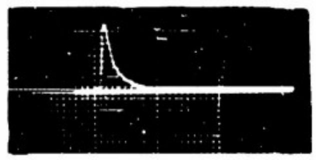
ONE-RETENTION

(THE OUTPUT SIGNAL FROM THE ARRAY UPON SELECTION OF CORE 00 — AFTER A NUMBER OF READ CYCLES AROUND THE REMAINING THREE CORES)

(d) AFTER 0 READ CYCLES



(e) AFTER 50 READ CYCLES



(f) AFTER 400 READ CYCLES

ZERO-RETENTION

(THE OUTPUT SIGNAL FROM THE ARRAY UPON SELECTION OF CORE 00 — AFTER A NUMBER OF WRITE-ONE CYCLES AROUND THE REMAINING THREE CORES)

EFFECTS OF DISTURBING ACTIVITY ON INFORMATION RETENTION

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F-1349

FIG. 5

Most of the deterioration of information occurs in the first few cycles of disturbing activity; as much reduction in the output of a ONE occurs during the first 50 cycles as during the following 350 cycles (compare a, b, and c of Figure 5); almost all of the increase in the output of a ZERO occurs in the first 50 cycles (d, e, and f). When the setup was operated by push button, there was no significant deterioration beyond 400 cycles of disturbing activity.

The disturbed-signal ratio, as taken on an area basis from Figure 5, is about 7; taken on an amplitude basis at 6 or 7 microseconds after the start of the pulses, it is much higher and becomes difficult to determine because the ZERO output has dropped by then to too low a value to measure.

Figure 6 indicates the results of using alternating-polarity sensing coils for the reduction of non-selecting noise. This noise is just the output from those cores which are in the same row or column as the selected core, and, consequently, receive half-value magnetizing-force pulses. When the windings are connected in series (aiding) the non-selecting pulses all add to the output from the selected core, the most serious effect being to increase the size of the ZERO output. The difference in amplitude of the ZERO output pulses (indicated by small arrows) is a measure of the effectiveness of alternating the polarities of sensing windings. The difference would be much larger in a large array.

One form of marginal check on the stability of operation of the array was made. It consisted of lowering and raising the amplitudes of the currents through the selecting windings, and observing signal ratios. It was found that all coordinate currents could be raised above an arbitrary optimum setting by 20% before signal ratios became marginal, and by 25% before the information patterns became completely unstable. Currents could be lowered to 20% below the optimum setting, at which point operation became unstable in the surrounding equipment and response times became about 35 microseconds. It was possible to hold the coordinate currents to within $\pm$ 5% of each other during these tests.

The main result of the preliminary tests on the four-core array is verification that the scheme of multi-coordinate storage and selection with magnetic cores is fundamentally sound. The unit is not as basic a tool as the single-core (coincident-current) tester, but it makes a fair demonstrator for the scheme. Design, development, and operation of a significantly larger array (at least 64 cores) is needed

(a) SERIES AIDING

(b) SERIES ALTERNATING

20 μs

PARTIAL CANCELLATION
OF NON-SELECTING NOISE

A-36885
F-1348

FIG. 6

in order to assess the ultimate practicability of arrays containing thousands of cores. Such work should be done on a design level aimed at Whirlwind standards in order to assure that pertinent problems will be uncovered and solved.

Signed................ W. N. Papian

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Approved.............. R. R. Everett

R. R. Everett

WNP:ap
Drawings:
A-50015
SB-36705-2
A-38999-G
A-36068
A-36886
A-36885